Keynote Speaker 3

Adam Crabb

Senior Business Development Manager, Grid Automation
GE Grid Solutions, China and East Asia Pacific

An Electrical Engineer with over 25 years' experience in wide range of fields and aspects within the Electricity Industry. Worked in Australian Utilities for 17 years in many roles with a strong focus on Substation Design (Primary and Secondary). Subsequently with AREVA/ Alstom/GE through the transitions in Sales, Technical Support and Project Delivery.

Focusing now on Business Development and bringing new Solutions to the Southeast Asia market utilising new technology, new application of established technology and combining the many facets of GE into a single optimised solution for the new challenges being faced in the Energy Industry.

Implementation of a system integrity protection scheme in the Channel Islands

Abstract: Channel Islands Electricity Grid (CIEG) is a company that is jointly owned by Jersey Electricity PLC (JE) and Guernsey Electricity Ltd (GEL). CIEG oversees the operation and management of several high-voltage electricity cables which connect the islands of Jersey and Guernsey to the electricity grid on mainland France, and by which electricity is imported into the islands. The connection to the French grid is through a 90 kV network operated by Reseau de Transport d'Electricite (RTE), France. In general, both systems were primarily developed to protect against faults or trip of on-island generating plant, and the possible need to trip (shed) customer load circuits to cover for the loss of generating capacity. As the CIEG grid has developed, a new scheme was required to protect the network against overload conditions. Such overload conditions may need to be removed by shedding of load on Jersey and Guernsey to prevent damage or cascade tripping. Circuit overload capabilities, both magnitude and duration, should be considered before any load-shedding actions are initiated. It was needed to design a system with the capability to respond and trip in <120 ms. The technical details adopted for the design of the SIPS are reported in this study.

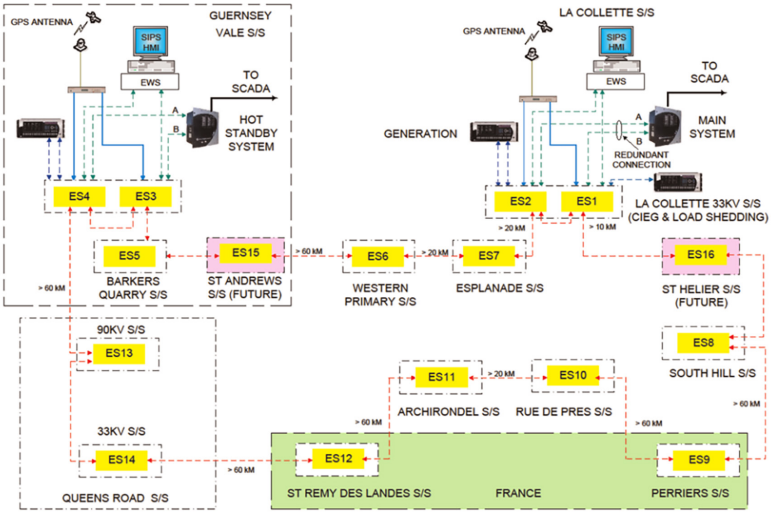

Fig1: Hardware architecture implemented